NOT RECOMMENDED FOR NEW DESIGNS
POSSIBLE SUBSTITUTE PRODUCT
INTERSIL PART NUMBER HIP4080A

February, 2003 FN3178.11

80V/2.5A Peak, High Frequency Full Bridge FET Driver

The HIP4080 is a high frequency, medium voltage Full Bridge N-Channel FET driver IC, available in 20 lead plastic SOIC and DIP packages. The HIP4080 includes an input comparator, used to facilitate the "hysteresis" and PWM modes of operation. Its HEN (high enable) lead can force current to freewheel in the bottom two external power MOSFETs, maintaining the upper power MOSFETs off. Since it can switch at frequencies up to 1MHz, the HIP4080 is well suited for driving Voice Coil Motors, switching power amplifiers and power supplies.

HIP4080 can also drive medium voltage brush motors, and two HIP4080s can be used to drive high performance stepper motors, since the short minimum "on-time" can provide fine micro-stepping capability.

Short propagation delays of approximately 55ns maximizes control loop crossover frequencies and dead-times which can be adjusted to near zero to minimize distortion, resulting in precise control of the driven load.

The similar HIP4081 IC allows independent control of all 4 FETs in an Full Bridge configuration.

See also, Application Note AN9324 for the HIP4080.

Similar part, HIP4080A, includes under voltage circuitry which doesn't require the circuitry shown in Figure 30 of this data sheet.

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HIP4080IP	-40 to 85	20 Lead PDIP	E20.3
HIP4080IB	-40 to 85	20 Lead SOIC	M20.3

Features

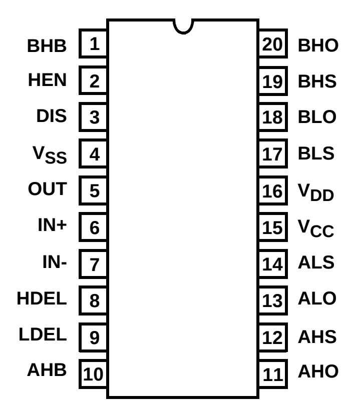
- Drives N-Channel FET Full Bridge Including High Side Chop Capability
- Bootstrap Supply Max Voltage to $95V_{DC}$
- Drives 1000pF Load at 1MHz in Free Air at 50^oC with Rise and Fall Times of 10ns (Typ)
- User-Programmable Dead Time
- Charge-Pump and Bootstrap Maintain Upper Bias Supplies
- DIS (Disable) Pin Pulls Gates Low
- Input Logic Thresholds Compatible with 5V to 15V Logic Levels
- Very Low Power Consumption

Applications

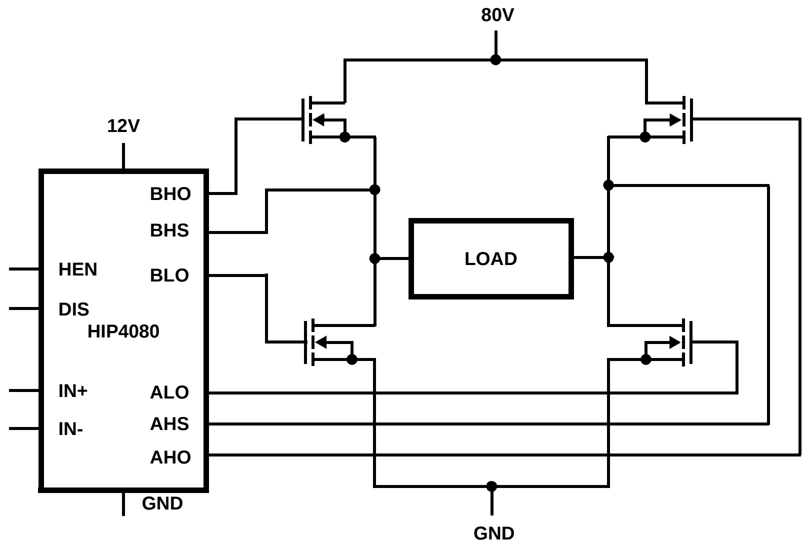
- Medium/Large Voice Coil Motors
- Full Bridge Power Supplies
- Switching Power Amplifiers
- High Performance Motor Controls
- Noise Cancellation Systems
- Battery Powered Vehicles
- Peripherals
- U.P.S.

Pinout

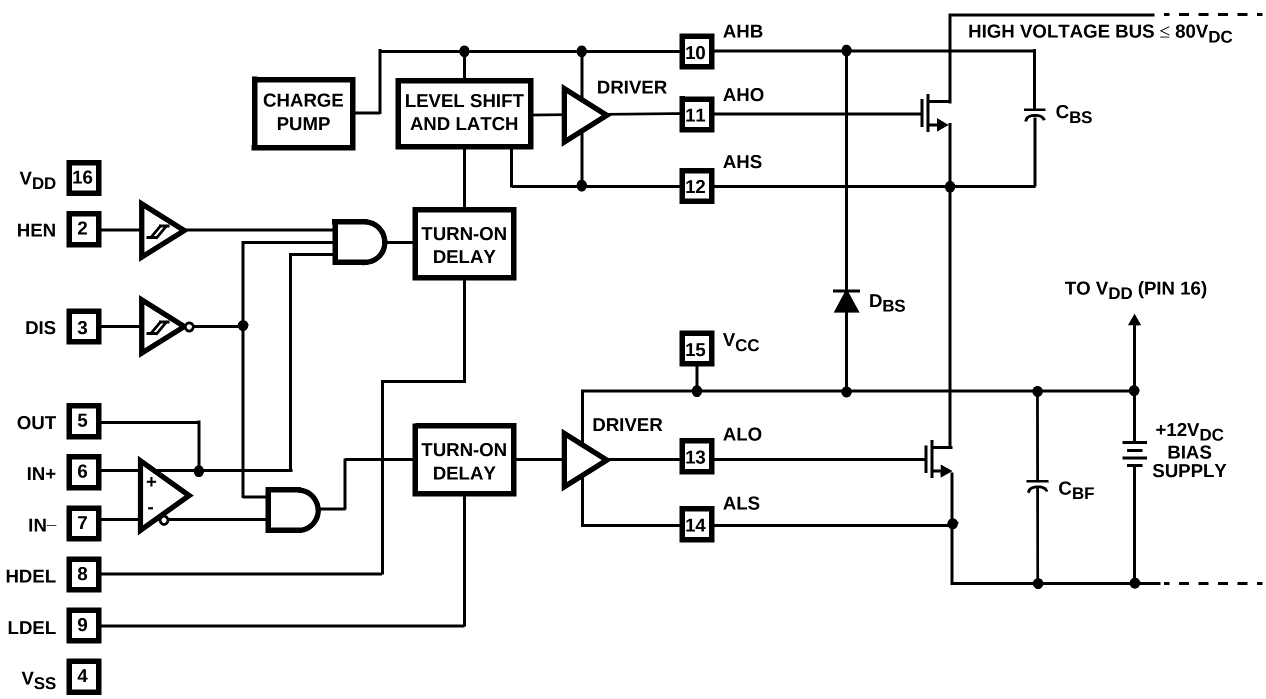
HIP4080
(20-LEAD PDIP, SOIC)
TOP VIEW



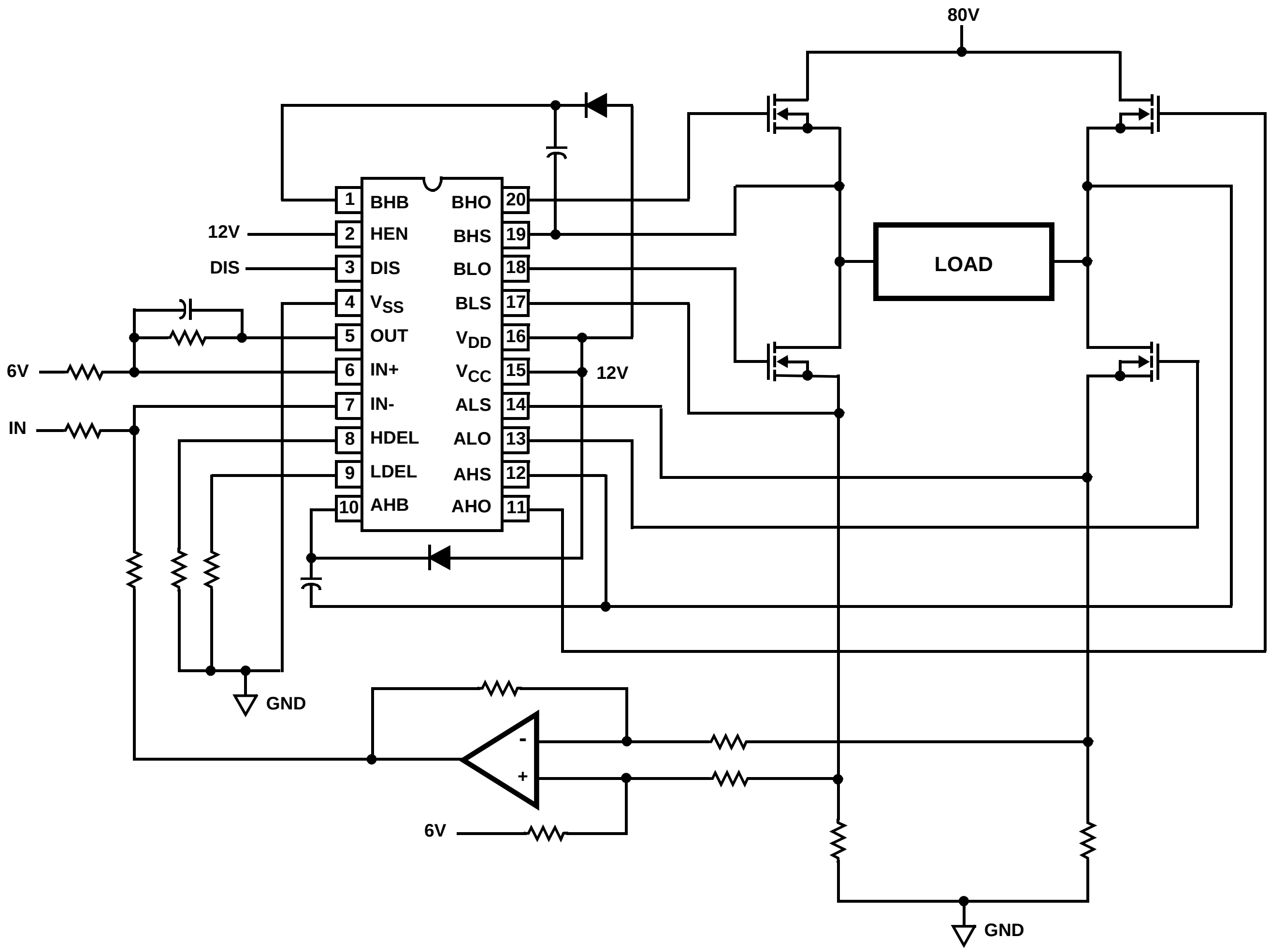
Application Block Diagram



Functional Block Diagram (1/2 HIP4080)



Typical Application (Hysteresis Mode Switching)



Absolute Maximum Ratings

Supply Voltage, V_{DD} and V_{CC} . . . . -0.3V to 16V
Logic I/O Voltages . . . . -0.3V to V_{DD} +0.3V
Voltage on AHS, BHS . . . -6.0V (Transient) to 80V (25^oC to 125^oC)
Voltage on AHS, BHS . . . -6.0V (Transient) to 70V (-55^oC to 125^oC
Voltage on ALS, BLS . . . . -2.0V (Transient) to +2.0V (Transient)
Voltage on AHB, BHB$V_{AHS, BHS}$ -0.3V to $V_{AHS, BHS}$ +16VVoltage on
Voltage on ALO, BLO . . . .$V_{ALS, BLS}$ -0.3V to V_{CC} +0.3V
Voltage on AHO, BHO. . . . . . $V_{AHS, BHS}$ -0.3V to $V_{AHB, BHB}$ +0.3V
Input Current, HDEL and LDEL . . . . -5mA to 0mA
Phase Slew Rate 20V/ns
All Voltages relative to pin 4, V_{SS}, unless otherwise specified.

Thermal Information

Thermal Resistance (Typical, Note 1). . . . . θ_{JA} (^oC/W)
SOIC Package. 85
PDIP Package 75
Maximum Power Dissipation at 85^oC
SOIC Package. 470mW
DIP Package 530mW
Storage Temperature Range . . . . -65^oC to 150^oC
Operating Max. Junction Temperature . . . . 125^oC
Lead Temperature (Soldering 10s) . . . . 300^oC
(SOIC - Lead Tips Only)

Operating Conditions

Supply Voltage, V_{DD} and V_{CC} . . . . +8V to +15V
Voltage on ALS, BLS. . . . . -1.0V to +1.0V
Voltage on AHB, BHB . . . . $V_{AHS, BHS}$ +5V to $V_{AHS, BHS}$ +15V
Input Current, HDEL and LDEL . . . . -500µA to -50µA
Operating Ambient Temperature Range . . . . -40^oC to 85^oC

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$V_{DD} = V_{CC} = V_{AHB} = V_{BHB}$ = 12V, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS}$ = 0V, $R_{HDEL} = R_{LDEL}$ = 100K, and $T_A = 25^oC$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	$T_J = 25^oC$			$T_J = -40^oC$ TO 125^oC		UNITS
			MIN	TYP	MAX	MIN	MAX	
SUPPLY CURRENTS AND CHARGE PUMPS								
V_{DD} Quiescent Current	I_{DD}	IN- = 2.5V, Other Inputs = 0V	8	10.5	13	7	14	mA
V_{DD} Operating Current	I_{DDO}	Outputs switching f = 500kHz	9	11	14	8	15	mA
V_{CC} Quiescent Current	I_{CC}	IN- = 2.5V, Other Inputs = 0V, $I_{ALO} = I_{BLO} = 0$	-	25	80	-	100	µA
V_{CC} Operating Current	I_{CCO}	f = 500kHz, No Load	1	1.5	2.0	0.8	3	mA
AHB, BHB Quiescent Current - Qpump Output Current	I_{AHB}, I_{BHB}	IN- = 2.5V, Other Inputs = 0V, $I_{AHO} = I_{BHO} = 0$, $V_{DD} = V_{CC} = V_{AHB} = V_{BHB}$ = 10V	-50	-30	-15	-60	-10	µA
AHB, BHB Operating Current	I_{AHBO}, I_{BHBO}	f = 500kHz, No Load	0.5	0.9	1.3	0.4	1.7	mA
AHS, BHS, AHB, BHB Leakage Current	I_{HLK}	$V_{AHS} = V_{BHS} = V_{AHB} = V_{BHB}$ = 95V	-	0.02	1.0	-	10	µA
AHB-AHS, BHB-BHS Qpump Output Voltage	V_{AHB} - V_{AHS} V_{BHB} - V_{BHS}	$I_{AHB} = I_{AHB}$ = 0, No Load	11.5	12.6	14.0	10.5	14.5	V
INPUT COMPARATOR PINS: IN+, IN-, OUT								
Offset Voltage	V_{OS}	Over Common Mode Voltage Range	-10	0	+10	-15	+15	mV
Input Bias Current	I_{IB}		0	0.5	2	0	4	µA
Input Offset Current	I_{OS}		-1	0	+1	-2	+2	µA
Input Common Mode Voltage Range	CMVR		1	-	V_{DD} -1.5	1	V_{DD} -1.5	V
Voltage Gain	AVOL		10	25	-	10	-	V/mV

Electrical Specifications

$V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} = 100K$, and $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	$T_J = 25^oC$ MIN	$T_J = 25^oC$ TYP	$T_J = 25^oC$ MAX	T_J = - 40°C TO 125°C MIN	T_J = - 40°C TO 125°C MAX	UNITS
OUT High Level Output Voltage	V_{OH}	IN+ > IN-, I_{OH} = -300μA	V_{DD} -0.4	-	-	V_{DD} - 0.5	-	V
OUT Low Level Output Voltage	V_{OL}	IN+ < IN-, I_{OL} = 300μA	-	-	0.3	-	0.4	V
High Level Output Current	I_{OH}	V_{OUT} = 6V	-9	-7	-4	-11	-2	mA
Low Level Output Current	I_{OL}	V_{OUT} = 6V	8	10	12	5	14	mA
INPUT PINS: DIS								
Low Level Input Voltage	V_{IL}	Full Operating Conditions	-	-	1.0	-	0.8	V
High Level Input Voltage	V_{IH}	Full Operating Conditions	2.5	-	-	2.7	-	V
Input Voltage Hysteresis			-	35	-	-	-	mV
Low Level Input Current	I_{IL}	V_{IN} = 0V, Full Operating Conditions	-130	-100	-75	-135	-65	μA
High Level Input Current	I_{IH}	V_{IN} = 5V, Full Operating Conditions	-1	-	+1	-10	+10	μA
INPUT PINS: HEN								
Low Level Input Voltage	V_{IL}	Full Operating Conditions	-	-	1.0	-	0.8	V
High Level Input Voltage	V_{IH}	Full Operating Conditions	2.5	-	-	2.7	-	V
Input Voltage Hysteresis			-	35	-	-	-	mV
Low Level Input Current	I_{IL}	V_{IN} = 0V, Full Operating Conditions	-260	-200	-150	-270	-130	μA
High Level Input Current	I_{IH}	V_{IN} = 5V, Full Operating Conditions	-1	-	+1	-10	+10	μA
TURN-ON DELAY PINS: LDEL AND HDEL								
LDEL, HDEL Voltage	V_{HDEL},V	$I_{HDEL} = I_{LDEL}$ = -100μA	4.9	5.1	5.3	4.8	5.4	V
GATE DRIVER OUTPUT PINS: ALO, BLO, AHO, AND BHO								
Low Level Output Voltage	V_{OL}	I_{OUT} = 100mA	.70	0.85	1.0	0.5	1.1	V
High Level Output Voltage	$V_{CC} - V_{OH}$	I_{OUT} = -100mA	0.8	0.95	1.1	0.5	1.2	V
Peak Pull-up Current	I_O+	V_{OUT} = 0V	1.7	2.6	3.8	1.4	4.1	A
Peak Pull-down Current	I_O-	V_{OUT} = 12V	1.7	2.4	3.3	1.3	3.6	A

Switching Specifications

$V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} = 10K$, C_L = 1000pF, and $T_A = 25^oC$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	$T_J = 25^oC$ MIN	$T_J = 25^oC$ TYP	$T_J = 25^oC$ MAX	T_J = - 40°C TO 125°C MIN	T_J = - 40°C TO 125°C MAX	UNITS
Lower Turn-off Propagation Delay (IN+/IN- to ALO/BLO)	T_{LPHL}		-	40	70	-	90	ns
Upper Turn-off Propagation Delay (IN+/IN- to AHO/BHO)	T_{HPHL}		-	50	80	-	110	ns
Lower Turn-on Propagation Delay (IN+/IN- to ALO/BLO)	T_{LPLH}	$R_{HDEL} = R_{LDEL}$ = 10K	-	45	70	-	90	ns
Upper Turn-on Propagation Delay (IN+/IN- to AHO/BHO)	T_{HPLH}	$R_{HDEL} = R_{LDEL}$ = 10K	-	70	110	-	140	ns
Rise Time	T_r		-	10	25	-	35	ns
Fall Time	T_f		-	10	25	-	35	ns
Turn-on Input Pulse Width	$T_{PWIN-ON}$	$R_{HDEL} = R_{LDEL}$ = 10K	50	-	-	50	-	ns
Turn-off Input Pulse Width	$T_{PWIN-OFF}$	$R_{HDEL} = R_{LDEL}$ = 10K	40	-	-	40	-	ns

Switching Specifications $V_{DD} = V_{CC} = V_{AHB} = V_{BHB}$ = 12V, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS}$ = 0V, $R_{HDEL} = R_{LDEL}$ = 10K, C_L = 1000pF, and $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	$T_J = 25^oC$			$T_J = -40^oC$ TO 125^oC		UNITS
			MIN	TYP	MAX	MIN	MAX	
Disable Turn-off Propagation Delay (DIS - Lower Outputs)	T_{DISLOW}		-	45	75	-	95	ns
Disable Turn-off Propagation Delay (DIS - Upper Outputs)	$T_{DISHIGH}$		-	55	85	-	105	ns
Disable to Lower Turn-on Propagation Delay (DIS - ALO and BLO)	T_{DLPLH}		-	35	70	-	90	ns
Refresh Pulse Width (ALO and BLO)	T_{REF-PW}		160	260	380	140	420	ns
Disable to Upper Enable (DIS - AHO and BHO)	T_{UEN}		-	335	500	-	550	ns
HEN-AHO, BHO Turn-off, Propagation Delay	$T_{HEN-PHL}$	$R_{HDEL} = R_{LDEL}$ = 10K	-	35	70	-	90	ns
HEN-AHO, BHO Turn-on, Propagation Delay	$T_{HEN-PLH}$	$R_{HDEL} = R_{LDEL}$ = 10K	-	60	90	-	110	ns

TRUTH TABLE

INPUT			OUTPUT			
IN+ > IN-	HEN	DIS	ALO	AHO	BLO	BHO
X	X	1	0	0	0	0
1	1	0	0	1	1	0
0	1	0	1	0	0	1
1	0	0	0	0	1	0
0	0	0	1	0	0	0

Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	BHB	B High-side Bootstrap supply. External bootstrap diode and capacitor are required. Connect cathode of bootstrap diode and positive side of bootstrap capacitor to this pin. Internal charge pump supplies 30μA out of this pin to maintain bootstrap supply. Internal circuitry clamps the bootstrap supply to approximately 12.8V.
2	HEN	High-side Enable input. Logic level input that when low overrides IN+/IN- (Pins 6 and 7) to put AHO and BHO drivers (Pins 11 and 20) in low output state. When HEN is high AHO and BHO are controlled by IN+/IN- inputs. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}).
3	DIS	DISable input. Logic level input that when taken high sets all four outputs low. DIS high overrides all other inputs. When DIS is taken low the outputs are controlled by the other inputs. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}).
4	V_{SS}	Chip negative supply, generally will be ground.
5	OUT	OUTput of the input control comparator. This output can be used for feedback and hysteresis.
6	IN+	Non-inverting input of control comparator. If IN+ is greater than IN- (Pin 7) then ALO and BHO are low level outputs and BLO and AHO are high level outputs. If IN+ is less than IN- then ALO and BHO are high level outputs and BLO and AHO are low level outputs. DIS (Pin 3) high level will override IN+/IN- control for all outputs. HEN (Pin 2) low level will override IN+/IN- control of AHO and BHO. When switching in four quadrant mode, dead time in a half bridge leg is controlled by HDEL and LDEL (Pins 8 and 9).
7	IN-	Inverting input of control comparator. See IN+ (Pin 6) description.
8	HDEL	High-side turn-on DELay. Connect resistor from this pin to V_{SS} to set timing current that defines the turn-on delay of both high-side drivers. The low-side drivers turn-off with no adjustable delay, so the HDEL resistor guarantees no shoot-through by delaying the turn-on of the high-side drivers. HDEL reference voltage is approximately 5.1V.

Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	DESCRIPTION
9	LDEL	Low-side turn-on DELay. Connect resistor from this pin to V_{SS} to set timing current that defines the turn-on delay of both low-side drivers. The high-side drivers turn-off with no adjustable delay, so the LDEL resistor guarantees no shoot-through by delaying the turn-on of the low-side drivers. LDEL reference voltage is approximately 5.1V.
10	AHB	A High-side Bootstrap supply. External bootstrap diode and capacitor are required. Connect cathode of bootstrap diode and positive side of bootstrap capacitor to this pin. Internal charge pump supplies 30μA out of this pin to maintain bootstrap supply. Internal circuitry clamps the bootstrap supply to approximately 12.8V.
11	AHO	A High-side Output. Connect to gate of A High-side power MOSFET.
12	AHS	A High-side Source connection. Connect to source of A High-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
13	ALO	A Low-side Output. Connect to gate of A Low-side power MOSFET.
14	ALS	A Low-side Source connection. Connect to source of A Low-side power MOSFET.
15	V_{CC}	Positive supply to gate drivers. Must be same potential as V_{DD} (Pin 16). Connect to anodes of two bootstrap diodes.
16	V_{DD}	Positive supply to lower gate drivers. Must be same potential as V_{CC} (Pin 15). De-couple this pin to V_{SS} (Pin 4).
17	BLS	B Low-side Source connection. Connect to source of B Low-side power MOSFET.
18	BLO	B Low-side Output. Connect to gate of B Low-side power MOSFET.
19	BHS	B High-side Source connection. Connect to source of B High-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
20	BHO	B High-side Output. Connect to gate of B High-side power MOSFET.

Timing Diagrams

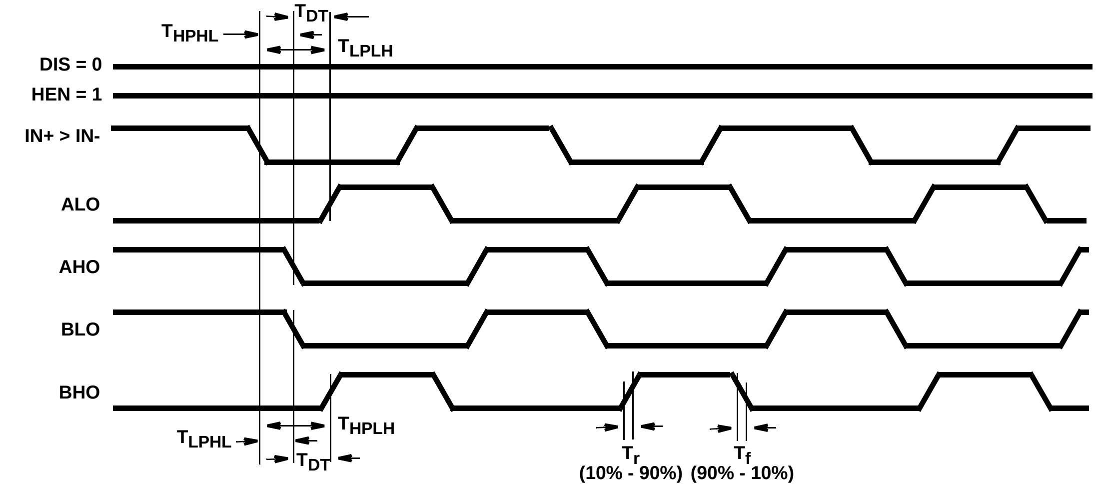


FIGURE 1. BI-STATE MODE

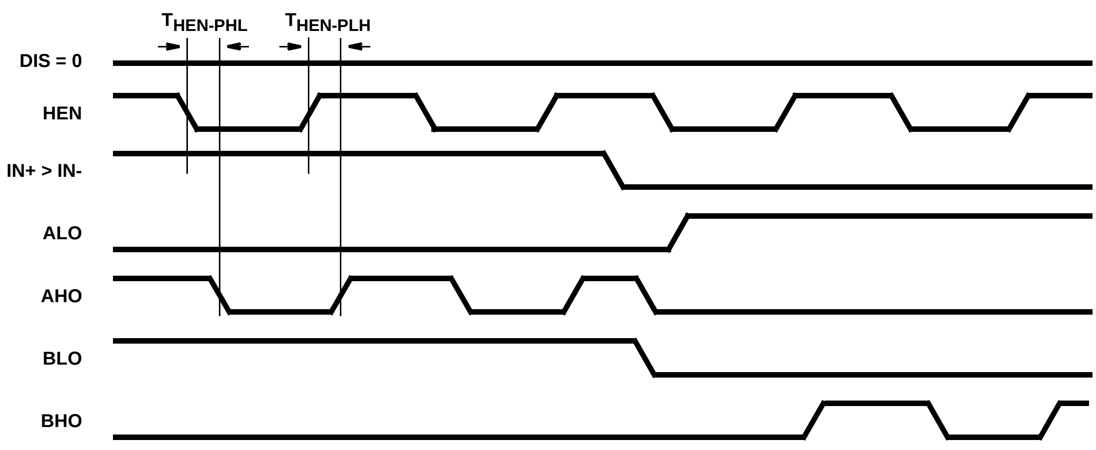


FIGURE 2. HIGH SIDE CHOP MODE

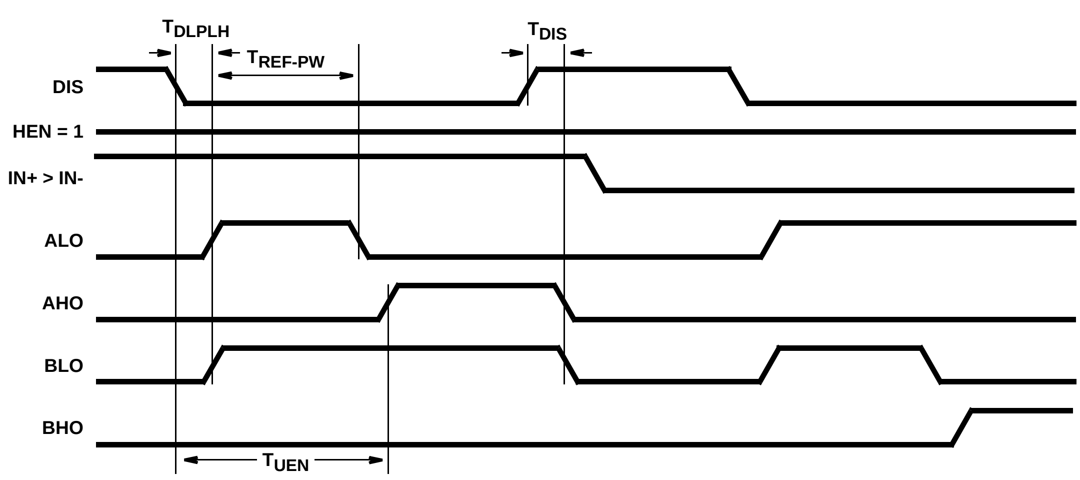


FIGURE 3. DISABLE FUNCTION

Typical Performance Curves $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} = 100K$, and $T_A = 25^oC$, Unless Otherwise Specified

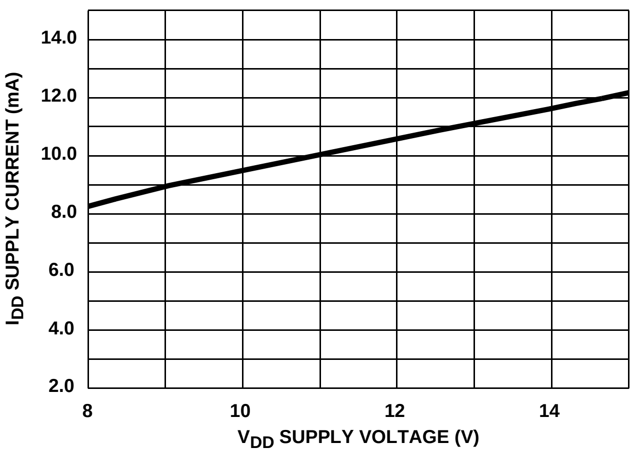


FIGURE 4. QUIESCENT I_{DD} SUPPLY CURRENT vs V_{DD} SUPPLY VOLTAGE

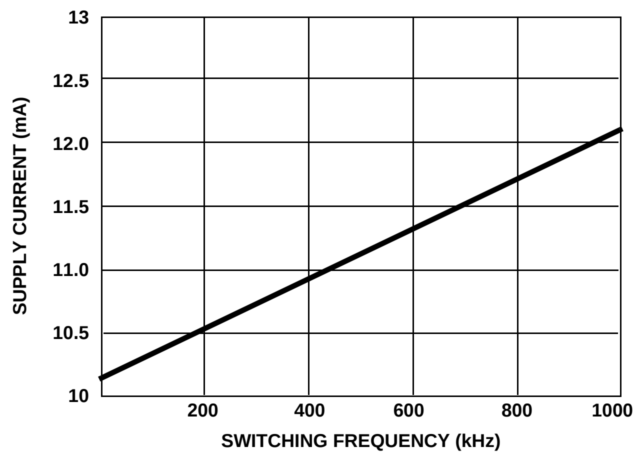


FIGURE 5. I_{DDO}, NO-LOAD I_{DD} SUPPLY CURRENT vs FREQUENCY (kHz)

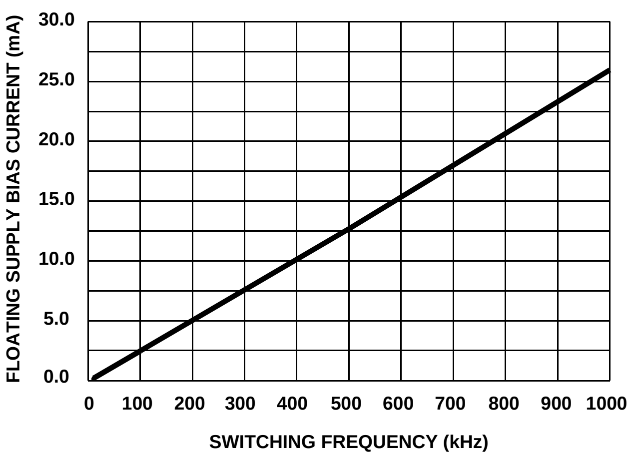


FIGURE 6. SIDE A, B FLOATING SUPPLY BIAS CURRENT vs FREQUENCY (LOAD = 1000pF)

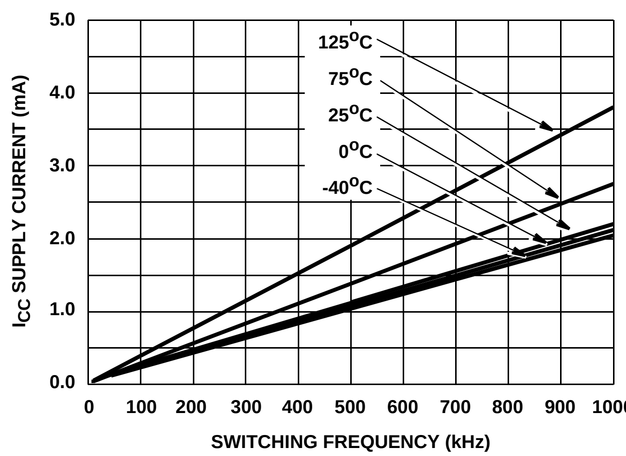


FIGURE 7. I_{CCO}, NO-LOAD I_{CC} SUPPLY CURRENT vs FREQUENCY (kHz) TEMPERATURE

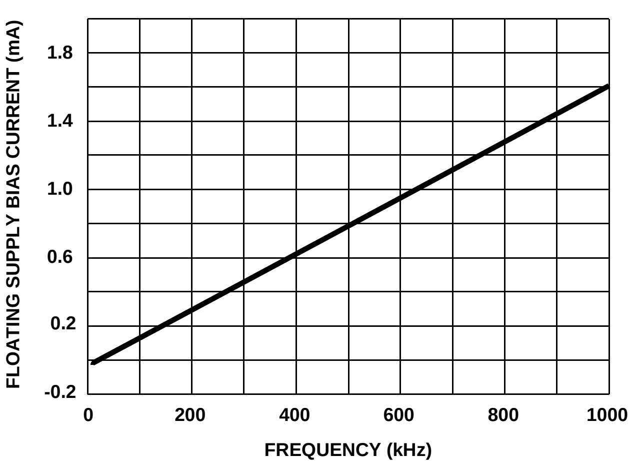


FIGURE 8. I_{AHB}, I_{BHB}, NO-LOAD FLOATING SUPPLY BIAS CURRENT vs FREQUENCY

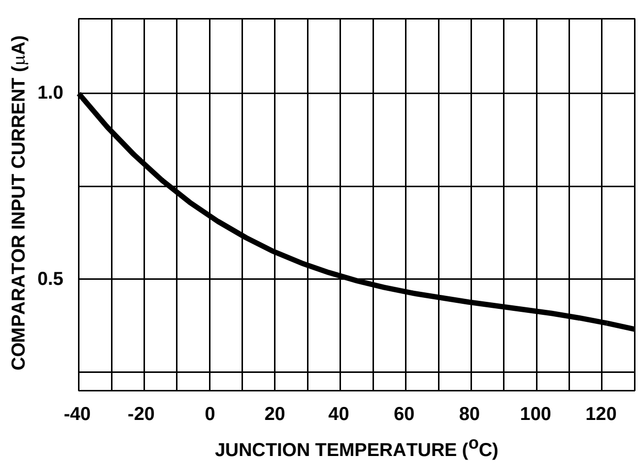


FIGURE 9. COMPARATOR INPUT CURRENT I_L vs TEMPERATURE AT V_{CM} = 5V

Typical Performance Curves $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} = 100K$, and $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

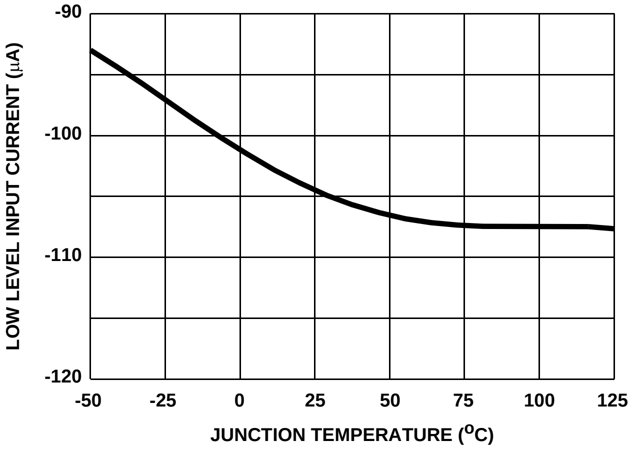


FIGURE 10. DIS LOW LEVEL INPUT CURRENT I_{IL} vs TEMPERATURE

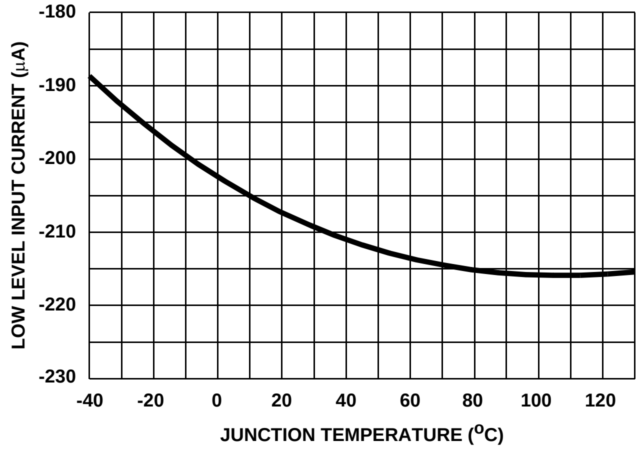


FIGURE 11. HEN LOW LEVEL INPUT CURRENT I_{IL} vs TEMPERATURE

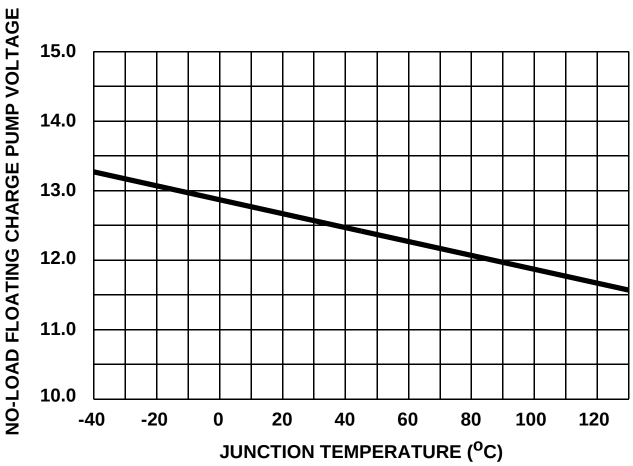


FIGURE 12. AHB - AHS, BHB - BHS NO-LOAD CHARGE PUMP VOLTAGE vs TEMPERATURE

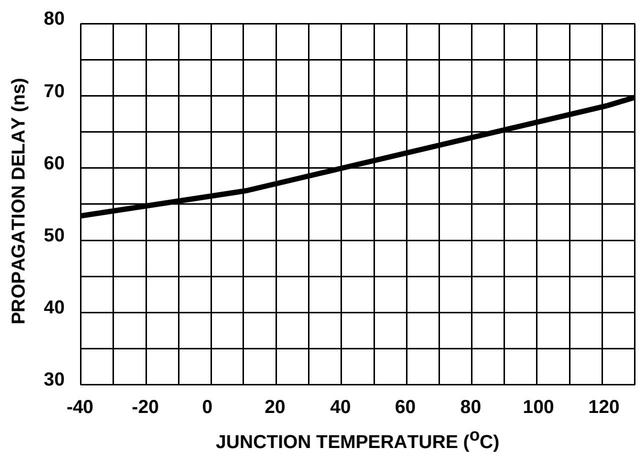


FIGURE 13. UPPER DISABLE TURN-OFF PROPAGATION DELAY $T_{DISHIGH}$ vs TEMPERATURE

Typical Performance Curves

$V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} = 100K$, and $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

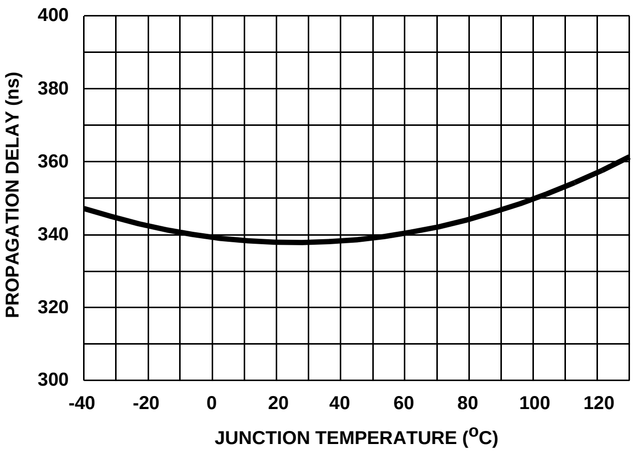


FIGURE 14. DISABLE TO UPPER ENABLE T_{UEN} PROPAGATION DELAY vs TEMPERATURE

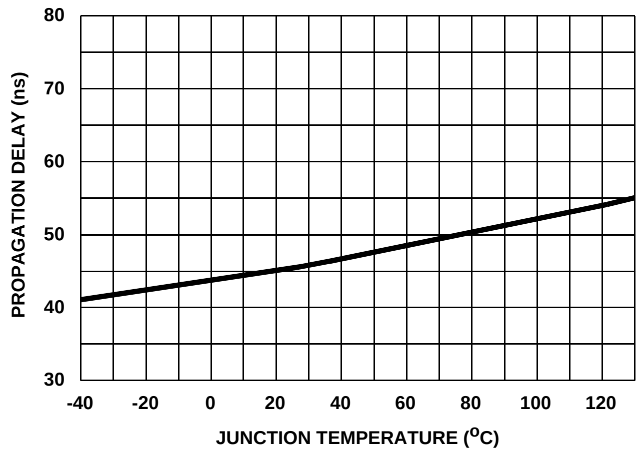


FIGURE 15. LOWER DISABLE TURN-OFF PROPAGATION DELAY T_{DISLOW} vs TEMPERATURE

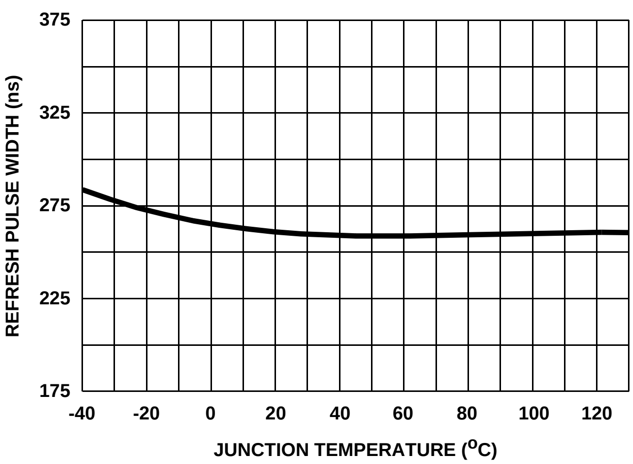


FIGURE 16. T_{REF-PW} REFRESH PULSE WIDTH vs TEMPERATURE

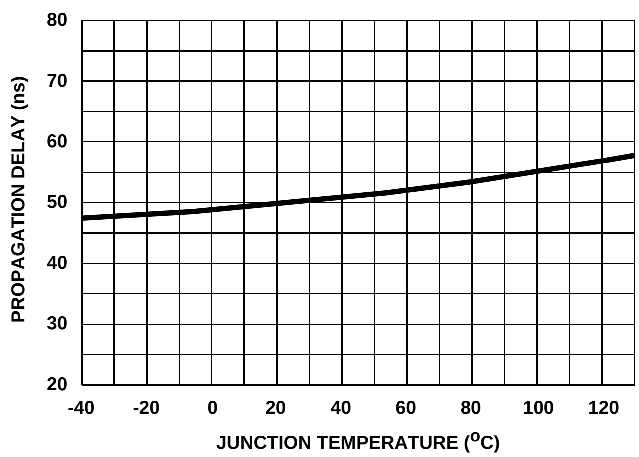


FIGURE 17. DISABLE TO LOWER ENABLE T_{DLPLH} PROPAGATION DELAY vs TEMPERATURE

Typical Performance Curves
$V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} = 100K$, and $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

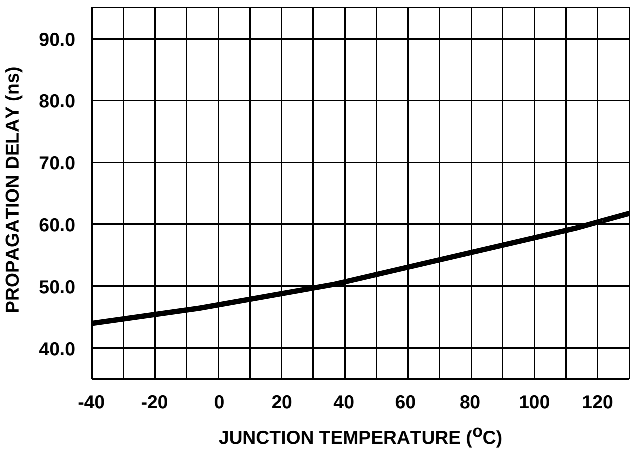


FIGURE 18. UPPER TURN-OFF PROPAGATION DELAY T_{HPHL} vs TEMPERATURE

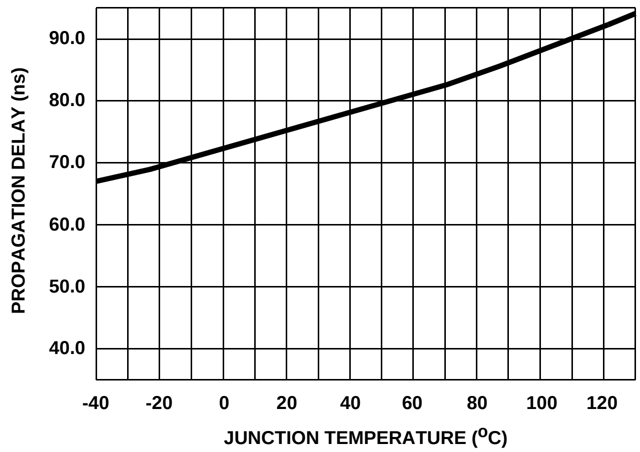


FIGURE 19. UPPER TURN-ON PROPAGATION DELAY T_{HPLH} vs TEMPERATURE

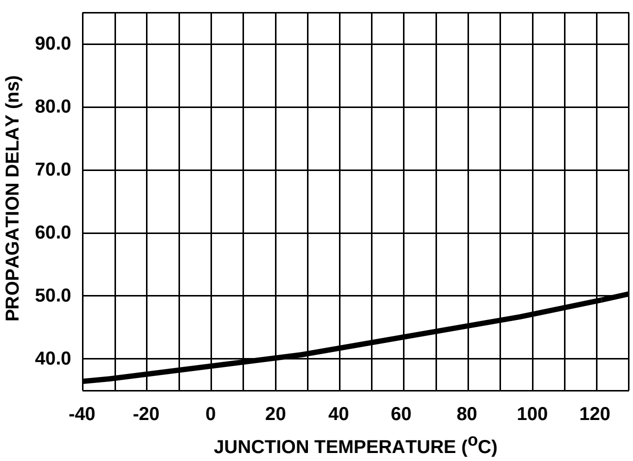


FIGURE 20. LOWER TURN-OFF PROPAGATION DELAY T_{LPHL} vs TEMPERATURE

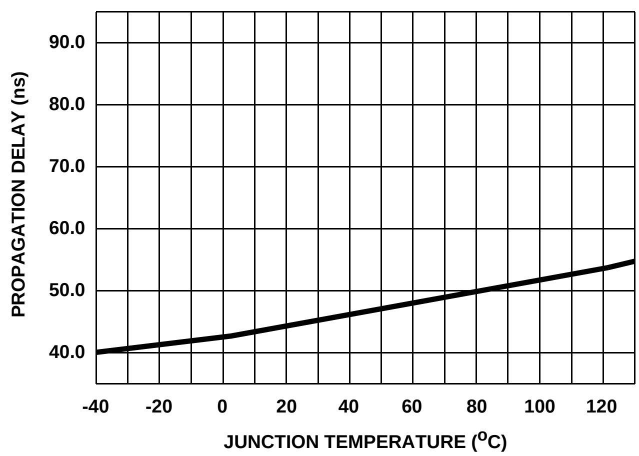


FIGURE 21. LOWER TURN-ON PROPAGATION DELAY T_{LPLH} vs TEMPERATURE

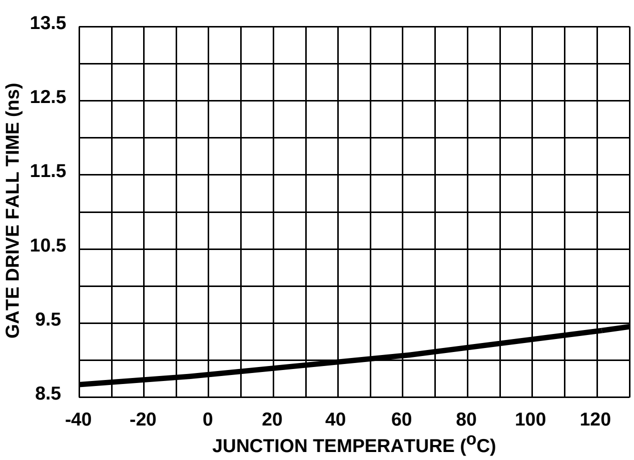


FIGURE 22. GATE DRIVE FALL TIME T_F vs TEMPERATURE

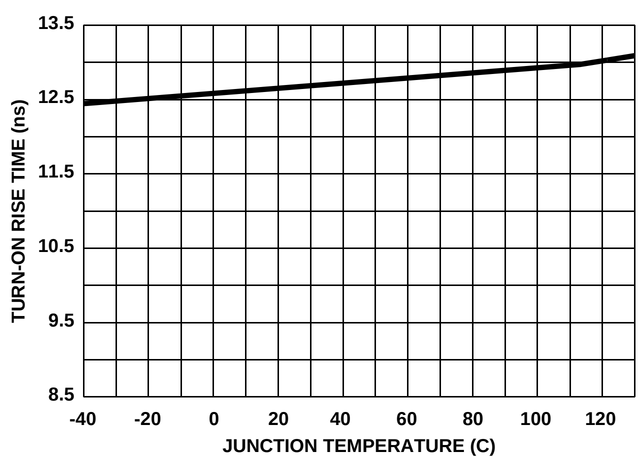


FIGURE 23. GATE DRIVE RISE TIME T_R vs TEMPERATURE

Typical Performance Curves $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} = 100K$, and $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

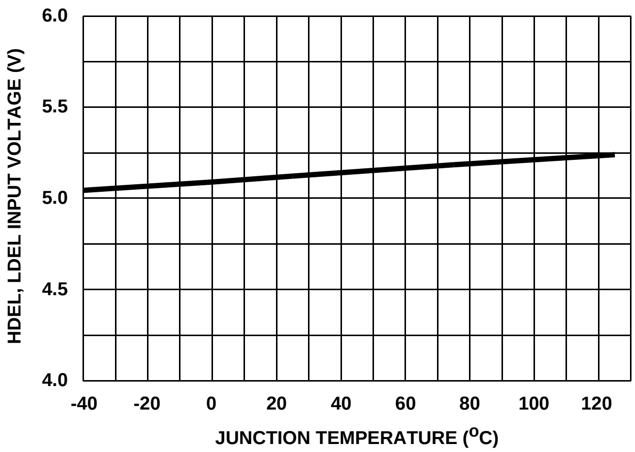


FIGURE 24. V_{LDEL}, V_{HDEL} VOLTAGE vs TEMPERATURE

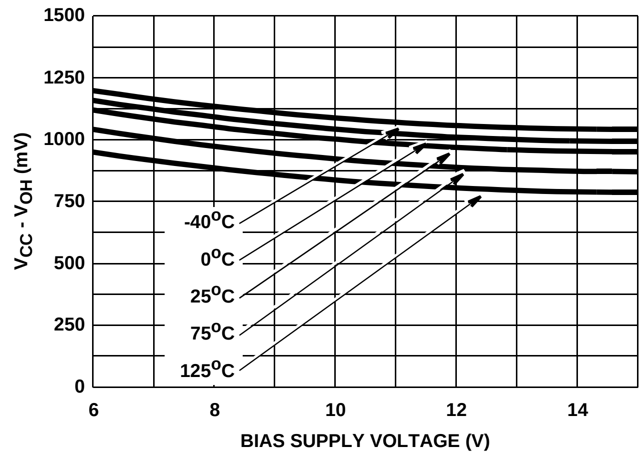


FIGURE 25. HIGH LEVEL OUTPUT VOLTAGE, V_{CC} - V_{OH} vs BIAS SUPPLY AND TEMPERATURE AT 100mA

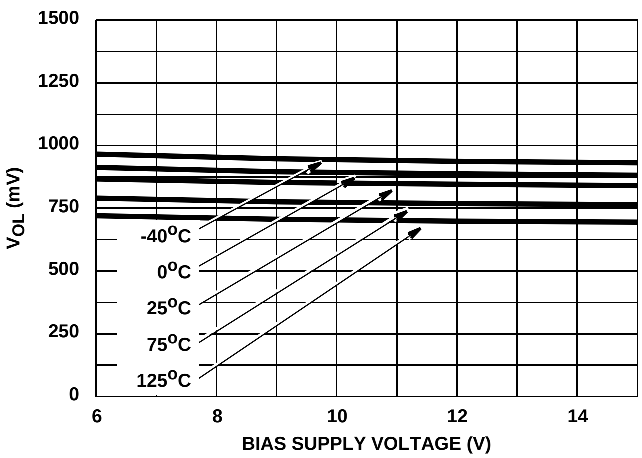


FIGURE 26. LOW LEVEL OUTPUT VOLTAGE V_{OL} vs BIAS SUPPLY AND TEMPERATURE AT 100mA

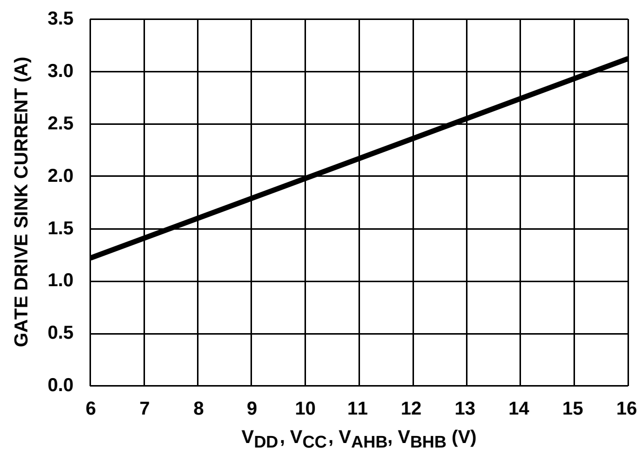


FIGURE 27. PEAK PULLDOWN CURRENT I_O vs BIAS SUPPLY VOLTAGE

Typical Performance Curves $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} = 100K$, and $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

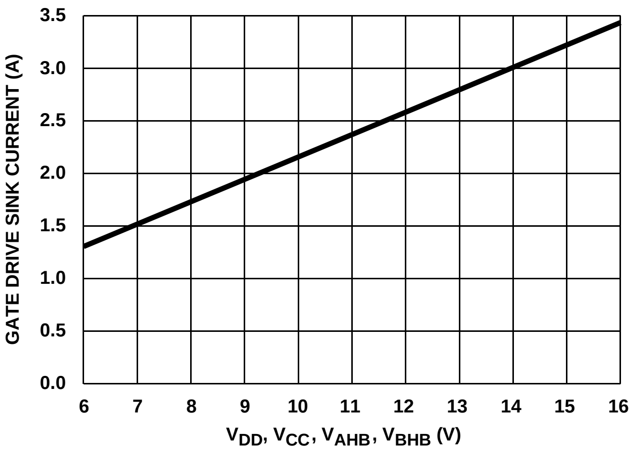


FIGURE 28. PEAK PULLUP CURRENT I_{O+} vs SUPPLY VOLTAGE

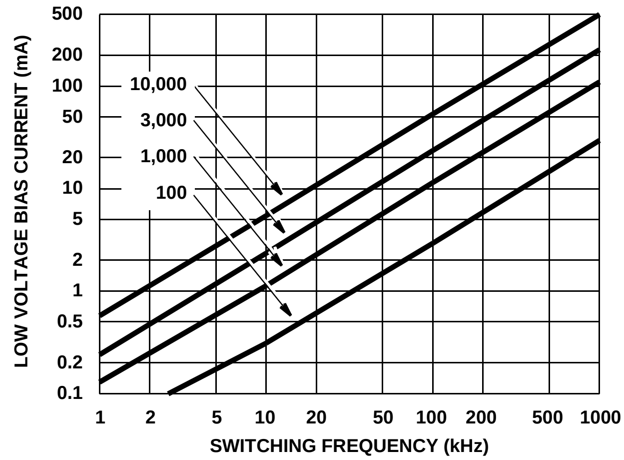


FIGURE 29. LOW VOLTAGE BIAS CURRENT I_{DD} AND I_{CC} (LESS QUIESCENT COMPONENT) vs FREQUENCY AND GATE LOAD CAPACITANCE

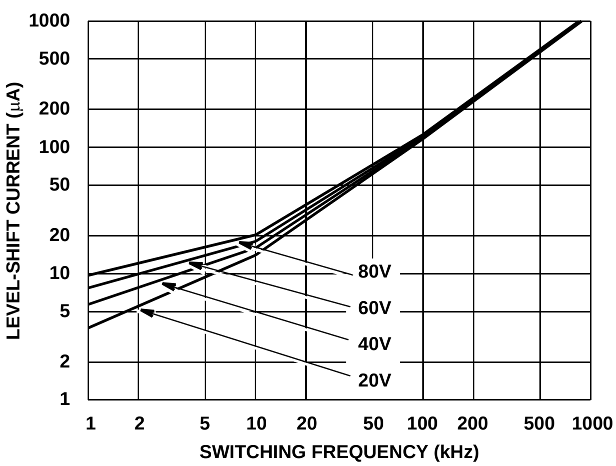


FIGURE 30. HIGH VOLTAGE LEVEL-SHIFT CURRENT vs FREQUENCY AND BUS VOLTAGE

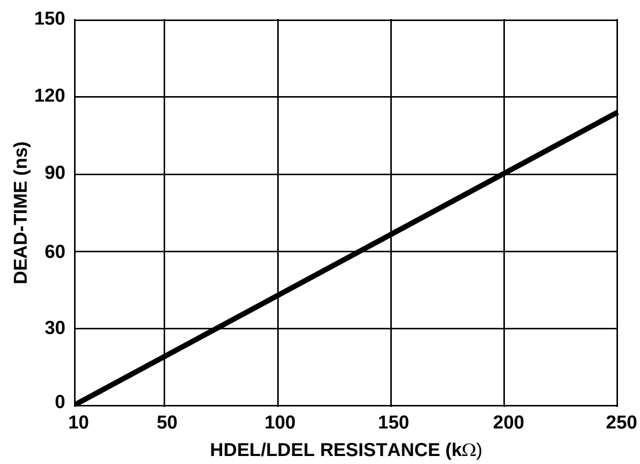


FIGURE 31. MINIMUM DEAD-TIME vs DEL RESISTANCE

HIP4080 Power-up Application Information

The HIP4080 H-Bridge Driver IC requires external circuitry to assure reliable start-up conditions of the upper drivers. If not addressed in the application, the H-Bridge power MOSFETs may be exposed to shoot-through current, possibly leading to MOSFET failure. Following the instructions below will result in reliable start-up.

The HIP4080 does not have an input protocol like the HIP4081 that keeps both lower power MOSFETs off other than through the DIS pin. IN+ and IN- are inputs to a comparator that control the bridge in such a way that only one of the lower power devices is on at a time, assuming DIS is low. However, keeping both lower MOSFETs off can be accomplished by controlling the lower turn-on delay pin, LDEL, while the chip is enabled, as shown in Figure 32. Pulling LDEL to V_{DD} will indefinitely delay the lower turn-on delays through the input comparator and will keep the lower MOSFETs off. With the lower MOSFETs off and the chip enabled, i.e. DIS = low, IN+ or IN- can be switched through a full cycle, properly setting the upper driver outputs. Once this is accomplished, LDEL is released to its normal operating point. It is critical that IN+/IN- switch a full cycle while LDEL is held high, to avoid shoot-through. This start-up procedure can be initiated by the supply voltage and/or the chip enable command by the circuit in Figure 32.

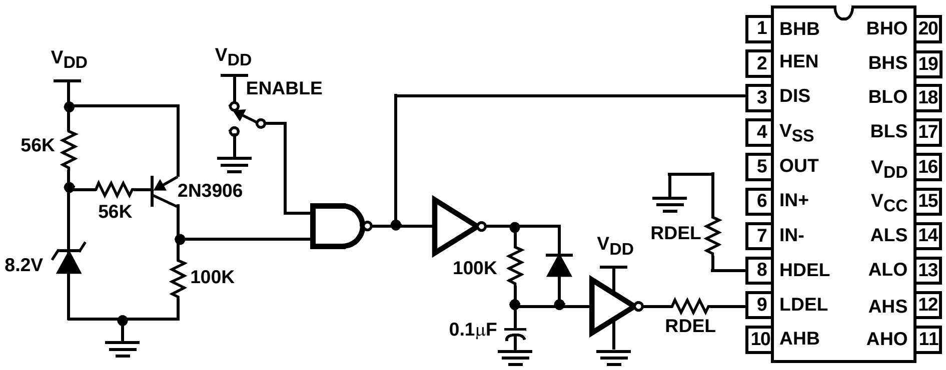
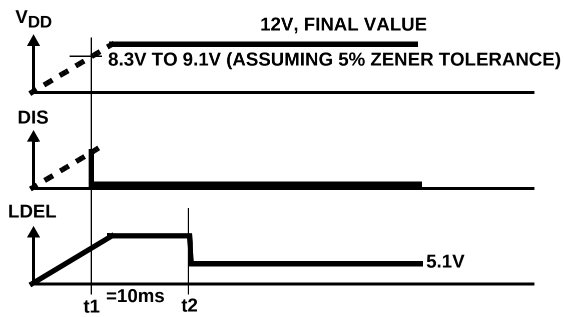


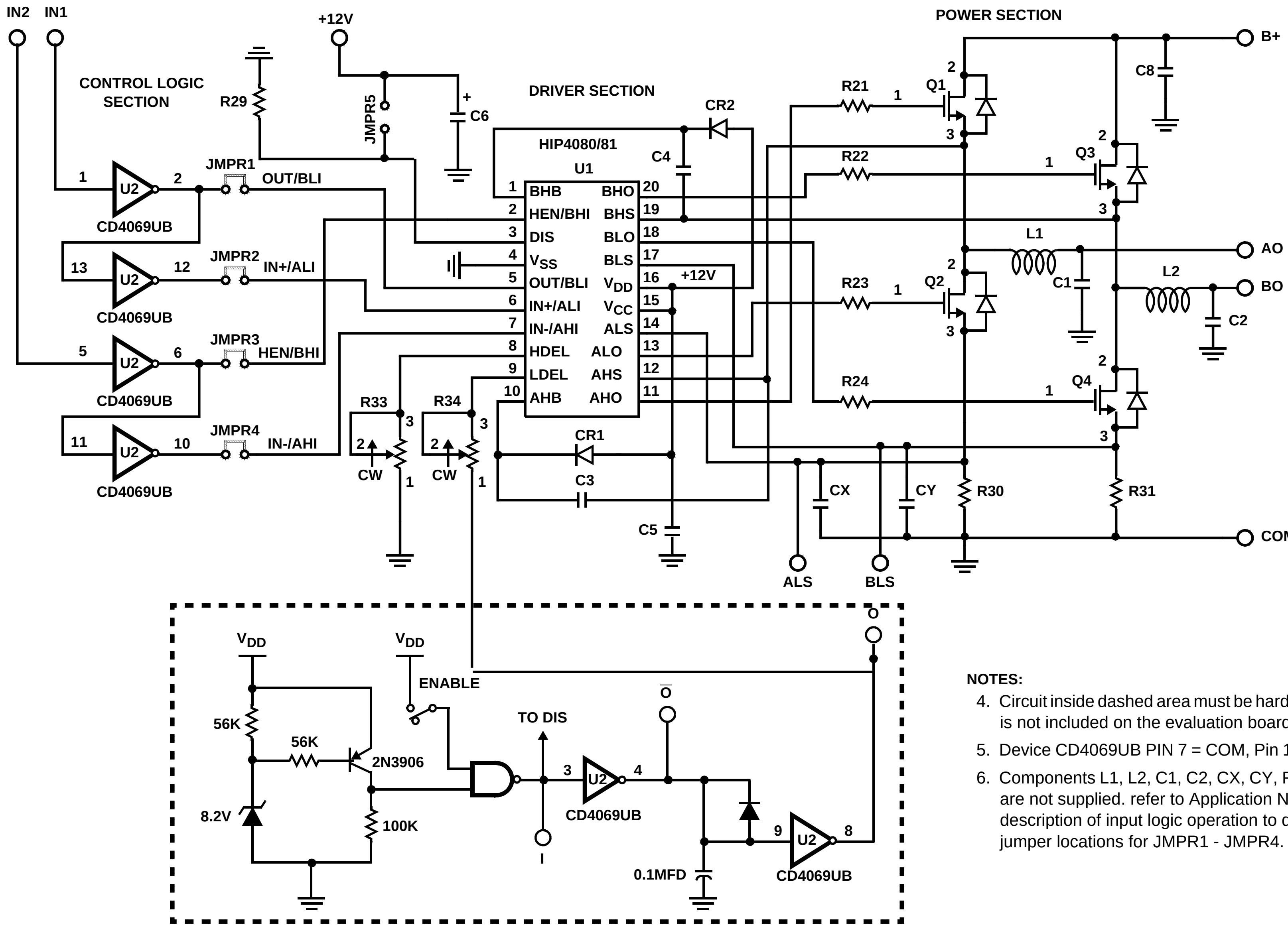
FIGURE 32.



NOTES:

2. Between t1 and t2 the IN+ and IN- inputs must cause the OUT pin to go through one complete cycle (transition order is not important). If the ENABLE pin is low after the under-voltage circuit is satisfied, the ENABLE pin will initiate the 10ms time delay during which the IN+ and IN- pins must cycle at least once.
3. Another product, HIP4080A, incorporates undervoltage circuitry which eliminates the need for the above power up circuitry.

FIGURE 33. TIMING DIAGRAM FOR FIGURE 32



NOTES:

4. Circuit inside dashed area must be hardwired and is not included on the evaluation board.
5. Device CD4069UB PIN 7 = COM, Pin 14 = +12V.
6. Components L1, L2, C1, C2, CX, CY, R30, R31, are not supplied. refer to Application Note for description of input logic operation to determine jumper locations for JMPR1 - JMPR4.

FIGURE 34. HIP4080 EVALUATION PC BOARD SCHEMATIC

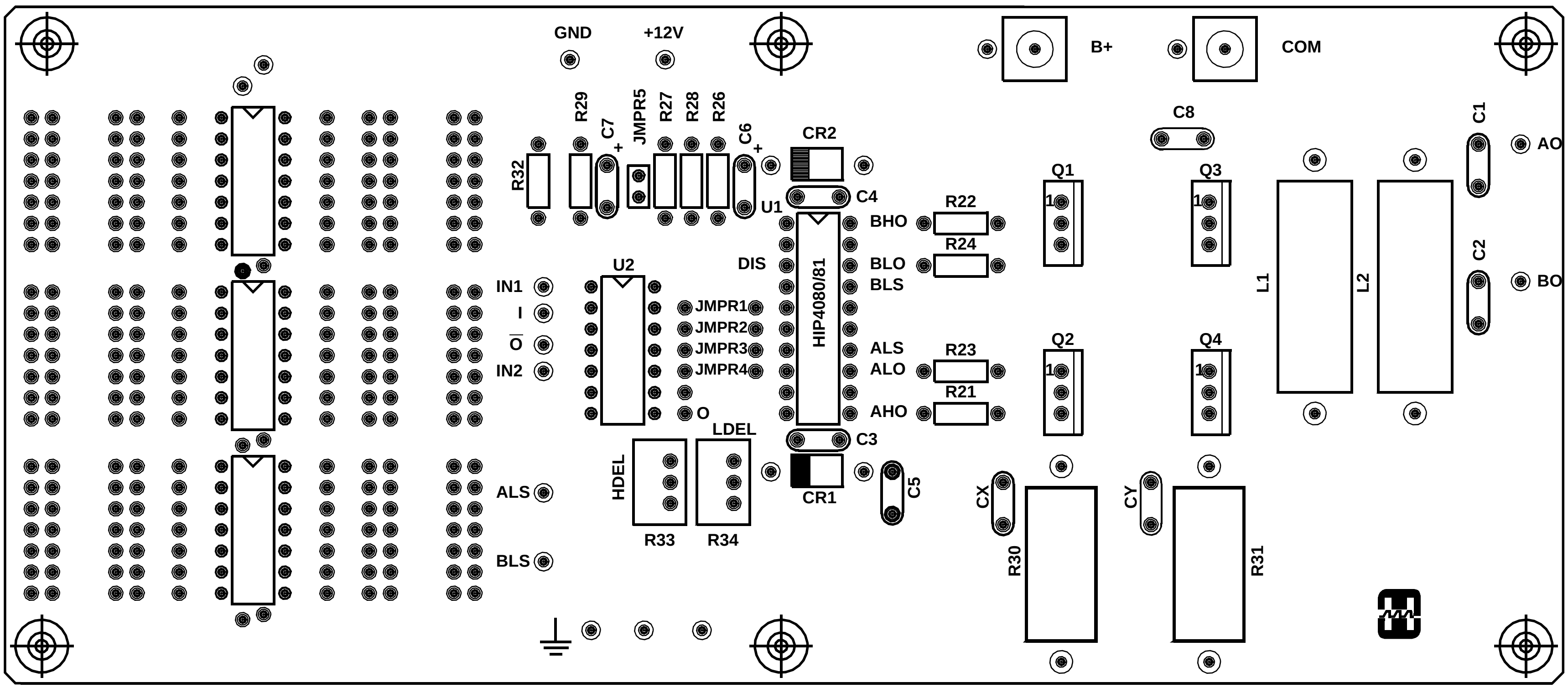


FIGURE 35. HIP4080 EVALUATION BOARD SILKSCREEN

Supplemental Information for HIP4080 and HIP4081 Power-Up Application

The HIP4080 and HIP4081 H-Bridge Driver ICs require external circuitry to assure reliable start-up conditions of the upper drivers. If not addressed in the application, the H-bridge power MOSFETs may be exposed to shoot-through current, possibly leading to MOSFET failure. Following the instructions below will result in reliable start-up.

HIP4081

The HIP4081 has four inputs, one for each output. Outputs ALO and BLO are directly controlled by input ALI and BLI. By holding ALI and BLI low during start-up no shoot-through conditions can occur. To set the latches to the upper drivers such that the driver outputs, AHO and BHO, are off, the DIS pin must be toggled from low to high after power is applied. This is accomplished with a simple resistor divider, as shown below in Figure 36. As the V_{DD}/V_{CC} supply ramps from zero up, the DIS voltage is below its input threshold of 1.7V due to the R1/R2 resistor divider. When V_{DD}/V_{CC} exceeds approximately 9V to 10V, DIS becomes greater than the input threshold and the chip disables all outputs. It is critical that ALI and BLI be held low prior to DIS reaching its threshold level of 1.7V while V_{DD}/V_{CC} is ramping up, so that shoot through is avoided. After power is up the chip can be enabled by the ENABLE signal which pulls the DIS pin low.

HIP4080

The HIP4080 does not have an input protocol like the HIP4081 that keeps both lower power MOSFETs off other than through the DIS pin. IN+ and IN- are inputs to a comparator that control the bridge in such a way that only one of the lower power devices is on at a time, assuming DIS is low. However, keeping both lower MOSFETs off can be accomplished by controlling the lower turn-on delay pin, LDEL, while the chip is enabled, as shown in Figure 37. Pulling LDEL to V_{DD} will indefinitely delay the lower turn-on delays through the input comparator and will keep the lower MOSFETs off. With the lower MOSFETs off and the chip enabled, i.e., DIS = low, IN+ or IN- can be switched through a full cycle, properly setting the upper driver outputs. Once this is accomplished, LDEL is released to its normal operating point. It is critical that IN+/IN- switch a full cycle while LDEL is held high, to avoid shoot-through. This start-up procedure can be initiated by the supply voltage and/or the chip enable command by the circuit in Figure 37.

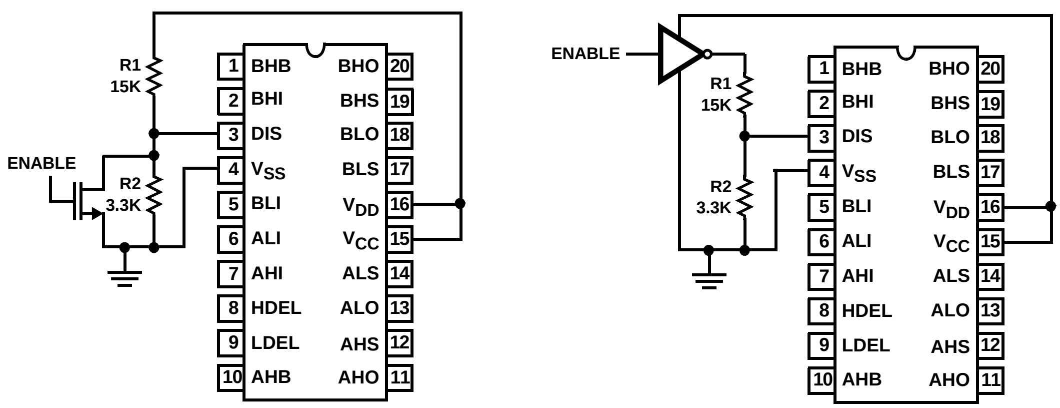


FIGURE 36.

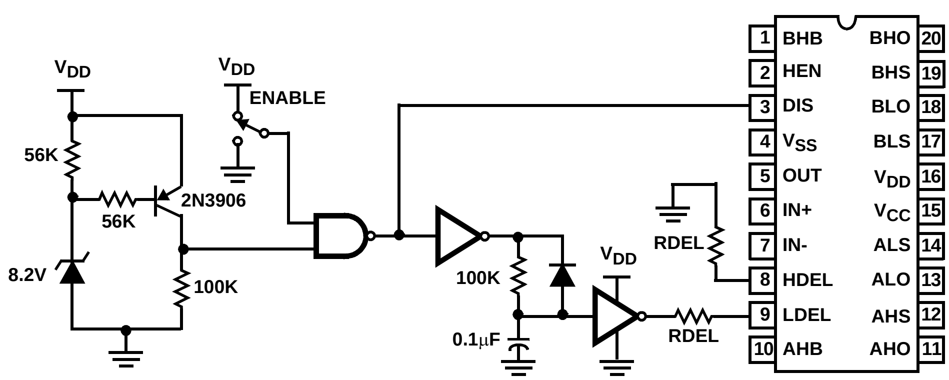
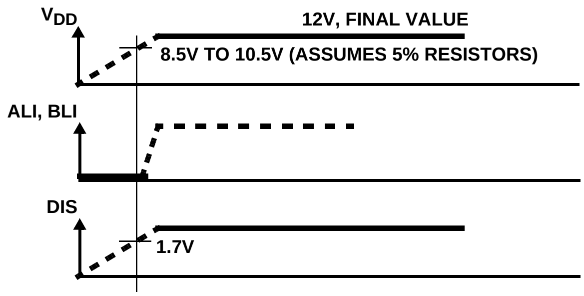


FIGURE 37.

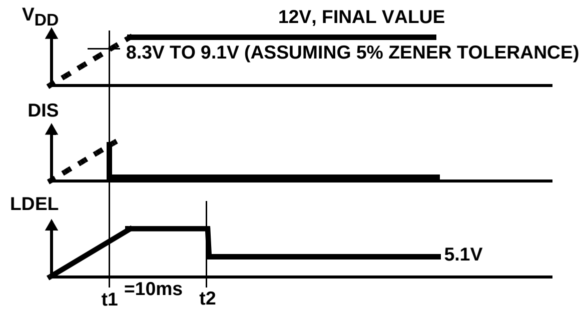
Timing Diagrams



NOTE:

7. ALI and/or BLI may be high after t1, whereupon the ENABLE pin may also be brought high.

FIGURE 38.

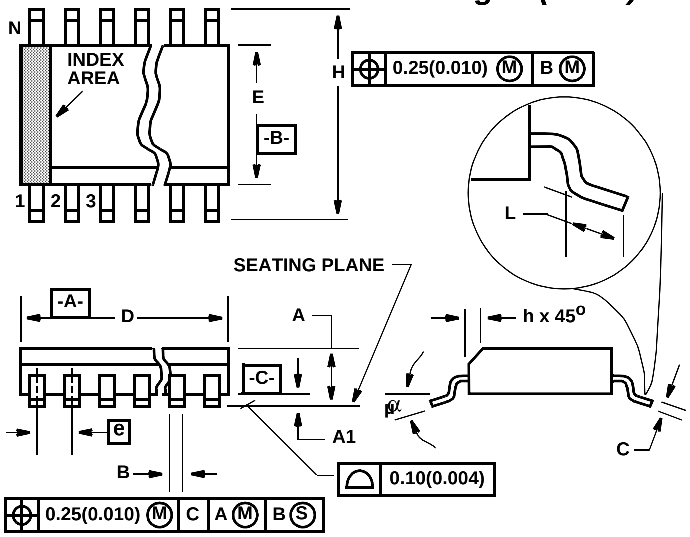


NOTE:

8. Between t1 and t2 the IN+ and IN- inputs must cause the OUT pin to go through one complete cycle (transition order is not important). If the ENABLE pin is low after the undervoltage circuit is satisfied, the ENABLE pin will initiate the 10ms time delay during which the IN+ and IN- pins must cycle at least once.

FIGURE 39.

Small Outline Plastic Packages (SOIC)



M20.3 (JEDEC MS-013-AC ISSUE C)
20 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.4961	0.5118	12.60	13.00	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
α	0°	8°	0°	8°	-

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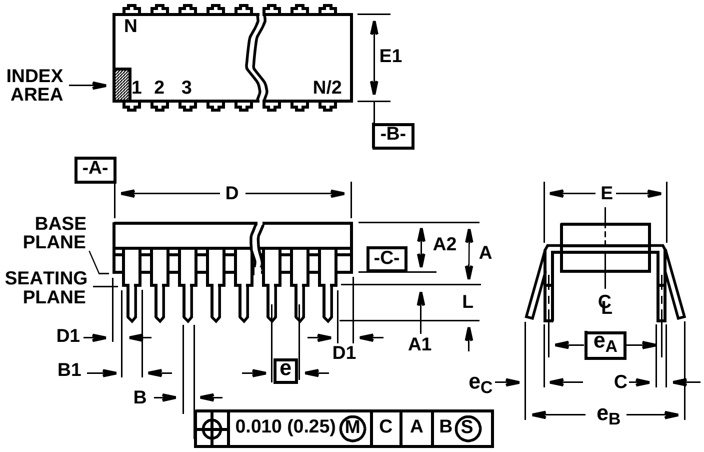
NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Dual-In-Line Plastic Packages (PDIP)



E20.3 (JEDEC MS-001-AD ISSUE D)
20 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.55	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.980	1.060	24.89	26.9	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	20		20		9

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NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C- .
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

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Intersil Corporation’s quality certifications can be viewed at www.intersil.com/design/quality

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